from the control input to output data at the provided address in the memory from the data output, and a readable port set to a status for identification and control of access to the memory, and (2) a connector for connecting the data input and the control input to the interface and supplying power to the external storage device, wherein the apparatus reads the status from the interface to identify access of the memory, and provides the control signal to the control input, and the address to the data input from the interface to output the data at the address in the memory from the data output.

42. (New) An apparatus having (1) an interface for data exchange from and to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein the storage device inputs a command from the data input in accordance with a control signal from the control input to output data in the memory from the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the storage device, wherein the apparatus provides the control signal to the control input from the interface, and the command to the data input from the interface to output data in the memory from the data output.

REMARKS

Claims 1, 2, 4-20, 22-29, and 31-38 are pending. By this amendment, claims 1, 4, 9, 19, 22, 23, 28 and 31 are amended, claims 39-42 are added, and claims 3, 21 and 30 are canceled. The attached appendix includes a marked-up copy of each rewritten claims(37 CFR 1.121 (1)(ii)). Claims 1, 4, 9, 19, 22, 23 and 31 are amended for clarity and consistency. And added claims 39-42 are rewritten from previous claim 28 and claims 31, 32, 35 and 39, respectively. Accordingly, no new matter is added by the above amendments.

Claims 1, 2, 4-20, 22-29, and 31-38 stand the rejection of double patenting over claims 1-2 of U.S. Patent No. 6,138,173, and the rejection is respectfully reversed.

As to independent claims 1, 19 and 28, claims 1-2 of U.S. Patent No. 6,138,173 do not disclose the storage device which "provides the data to the memory in accordance with a control signal from the control input to store the data at the provided address in the memory or to output data at the provided address in the memory to the data output". as recited in claims 1, 19 and 28, which store/output data in the provided address and are not slight variation. Therefore, the presenting claims 1-2 of U.S. Patent No. 6,138,173 do not cover the subject matter of claims 1, 19 and 28

in this application which have differrent subject matter.

Claims 1, 2, 4-20, 22-29, and 31-38 stand the rejections under 35 U.S.C.102(b) over Patent 4,225,498 to Schuller, and the rejection is respectfully reversed.

Schuller discloses a serial access memory which has a data input, a data output, a control input and memory elements, where data are input synchronous or asynchronous with respect to the clock, and the correct writing of the input data in a desired memory location to set the transition of the write enable signal (for example, col. 2 line 23 - col. 3 line 36). However, the serial access memory is provided address to the address input of ROM with Address Decorder (for example, Fig.1 and col. 2 line 23 - 29), so that Schuller does not disclose or suggest the storage device which "provides an address input from the data input to the memory" and "stores data provided to the data input at the address" in the memory.

Therefore, the independent claims and their dependent claims 1, 2, 4-20, 22-29, and 31-38 are patentable over the claims 1-2 of U.S. Patent No. 6,138,173 and Schuller.

Claims 39-42 stand the rejection of double patenting over claims 1-2 of U.S. Patent No. 6,138,173, and the rejection is respectfully reversed.

Claims 1-2 of U.S. Patent No. 6,138,173 do not disclose the storage device which has "a memory provided an address from the data input" as recited in claims 39-41, and do not disclose the storage device which "inputs a command from the data input" as recited in claim 42, which output data in the memory and are not slight variation. Therefore, the presenting claims 1-2 of U.S. Patent No. 6,138,173 do not cover the subject matter of claims 39-42 in this application which have differrent subject matter.

And claims 39-42 stand the rejections under 35 U.S.C.102(b) over Patent 4,225,498 to Schuller, and the rejection is respectfully reversed.

Schuller does not disclose or suggest any apparatus which provides "changed part of the address to the data input" as recited in claim 39, "sets a value into the interface" as recited in claim 40, has "a readable port set to a status" as recited in claim 41, or "inputs a command from the data input" as recited in claim 42.

Therefore, the independent claims 39-42 are patentable over the claims 1-2 of U.S. Patent No. 6,138,173 and Schuller.

Applicant submits the Information Disclosure Statement, in which the documents are informed to Applicant by Japanese Patent Office (JPO) on Aug. 18, 2004, where Foreign Priority Application of this application is now under examination.

The documents are downloaded from web-pages in the internet-cite of JPO, as follows:

As to JP A-7-175747, Disclosure and translation of Frontpage and Description,

As to JP A-7-28741, Disclosure and translation of Frontpage and Description,

As to JP A-7-56659, Disclosure and translation of Frontpage and Description,

As to JP U-6-25938, Disclosure and translation of Description,

As to JP A-3-241417, Disclosure and translation of Frontpage, and

As to JP A-63-29871, Disclosure and translation of Frontpage.

These documents are desired to be taken into consideration.

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe anything further would be desirable to place this application in even better condition for allowance.

Respectfully submitted,

Tadahiko Hisano

Signature: Tadahiko Hisano

Date : Sep. 01, 2004

Attachment:

Appendix

Information Disclosure Statement

APPENDIX

Changes to Claims:

Claims 3, 21, and 30 are canceled.

Claims 39-42 are added.

The following is a marked-up version of the amended claims:

1. (Amended) A storage device comprising:

a memory for storing data ;and

a circuit having a data input, a control input, and a data output;

wherein ~~the circuit provides data input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input in the memory or to output data stored in the memory to the data output~~ the circuit provides an address input from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the address in the memory or to output data at the address in the memory to the data output.

4. (Amended) The storage device according to claim ~~3~~1, wherein the circuit has ports for providing the data and the address to the memory and a data bus for transferring the data from the data input to one of the ports by the control signal of the control input.

9. (Amended) The storage device according to claim ~~3~~1, wherein the circuit inputs part of the address from the data input to set the part to selected bit of a held address that is modified by the part, and provides the modified address to the memory.

19. (Amended) A method for access to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein ~~the storage device inputs data from the data input, and provides the data to the memory in accordance with a control signal from the control input to store the data in the memory~~ the storage device provides an address from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the provided address in the memory or to output data at the address in the memory to the data output, comprising:

providing an address to the data input to output the address to the memory;

providing data to the data input to output the data to the memory; and

providing a first control signal to the control input to store the data at the address into the memory.

22. (Amended) The method according to claim ~~21~~19, further comprising:

providing an address to the data input to set the address of memory; and

providing a second control signal to the control input to output the data at the address in the memory to the data output.

23. (Amended) The method according to claim ~~21~~19, further comprising, providing part of the address to set the part to selected bits of an address held in the storage device for modifying the address and output the modified address to the memory.

28. (Amended) An apparatus having (1) an interface for data exchange from and to a storage device having a data input, a control input, a data output, and a memory for storing data, wherein ~~the storage device inputs data from the data input, provides the data to the memory in accordance with a control signal from the control input to store the data memory~~ the storage device provides an address from the data input to the memory in accordance with a control signal from the control input to store data provided to the data input at the provided address in the memory or to output data at the address in the memory to the data output, and (2) a connector for connecting the data input, a data output and the control input to the interface and supplying power to the storage device, wherein the apparatus provides the control signal to the control input from the interface, and the data or an address to the data input from the interface to store the data at the address in the memory or to output data at the address in the memory to the data output.

31. (Amended) The apparatus according to claim ~~30~~28, wherein the apparatus provides part of the address to the data input to set the part to selected bits of an address held in the storage device for modifying the address and output the modified address to the memory.